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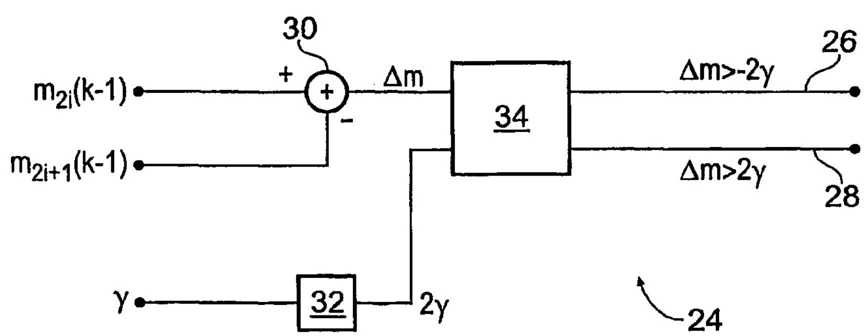
Declaration under Rule 4.17:
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACS APPARATUS AND METHOD FOR VITERBI DECODER



(57) **Abstract:** The circuit (10) performs a butterfly calculation for a Viterbi trellis by using two path metrics and a branch metric to generate two new path metrics. The new metrics are produced by adders (12) and (14) whose inputs are controlled by selectors (16-22). The outputs of the selectors (16-22) are controlled by selection control unit (24) which considers the difference between the given path metrics relative to the double of the branch metric, which represents a branch metric difference.

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3(4)

JC06 Rec'd PCT/PTO 28 OCT 2005

ACS APPARATUS AND METHOD FOR VITERBI DECODER

The invention relates to methods of, and apparatus for, the calculation of metrics for use in, for example, the decoding of convolutionally encoded signals.

A convolutionally encoded signal can be decoded using the Viterbi algorithm.

In a decoding process using the Viterbi algorithm, a received signal is represented as a trellis of states and path metrics are calculated recursively for the states in the trellis by using branch metrics to move between the states. Figure 1 illustrates a butterfly calculation showing how, in Viterbi decoding, path metrics m_i and $m_{i+N/2}$ are calculated for the k^{th} stage of a trellis from path metrics m_{2i} and m_{2i+1} of the $k-1^{th}$ stage of the trellis using the branch metric γ between the k^{th} and the $k-1^{th}$ stages. As is well known, each of the k^{th} stage path metrics calculated in the illustrated butterfly calculation is determined using two $k-1^{th}$ stage path metrics in an add/compare/select (ACS) operation.

One aim of the invention is to improve the manner in which ACS operations are performed.

According to one aspect, the invention provides a method of calculating a first new path metric from two old path metrics and a branch metric, the method comprising: determining the difference between the two old path metrics; performing a first comparison of the branch metric and said difference; selecting, on the basis of said first comparison, one of the old path metrics for a first combination with the branch metric; and selecting, on the basis of said first comparison, whether said first combination is by addition or subtraction.

The invention also consists in apparatus for calculating a first new path metric from two old path metrics and a branch metric, the apparatus comprising: subtracting means for determining the difference between the old path metrics; comparing means for performing a first comparison of the branch metric and said difference; and selecting means for selecting, on the basis of said first comparison, one of the old path metrics for a first

combination with the branch metric and for selecting, on the basis of said first comparison, whether said first combination is by addition or subtraction.

By calculating path metrics in this fashion, relatively few operations are required thus providing the possibilities of enhancing the speed of operation of, and reducing the silicon area required for, hardware that is configured to calculate path metrics.

In certain embodiments, a second new path metric is calculated from the old path metrics and the branch metric on the basis of a second comparison of the branch metric with the difference in the old path metrics.

In some embodiments, the comparison that controls the calculation of a new path metric is the determination of which is the larger of the difference in the old path metrics and double the branch metric or which is the larger of the difference in the old path metrics and minus double the branch metric.

In some embodiments, comparisons between the difference in the old path metrics and the branch metric involve inspecting the signs of the quantities to be compared to see if the result of the comparison can be deduced from said signs or whether the result of the comparison needs to be calculated from said difference and said branch metric.

The invention is also applicable to decoding schemes other than the Viterbi algorithm, where butterfly calculations may be used. For example, the invention can be used in log-MAP decoding processes.

From a further perspective, the invention also relates to computer programmes, conveyed on a suitable storage device or otherwise, for performing metric calculation methods according to the invention.

By way of example only, an embodiment of the invention will now be described with reference to the accompanying figures, in which:

Figure 1 illustrates metric calculations forming a butterfly calculation;

Figure 2 illustrates a circuit for performing ACS operations;

Figure 3 illustrates the selector control unit of the circuit of Figure 2 in more detail;

Figure 4 illustrates the comparison unit of Figure 3 in more detail; and

Figure 5 illustrates an alternative circuit that can be used for the comparison unit of Figure 3.

In Figure 1, $m_i(k)$ is the greater of $[m_{2i}(k-1)+\gamma]$ and $[m_{2i+1}(k-1)-\gamma]$. The condition of the former quantity being greater than the latter can be expressed as the inequality:

$$m_{2i}(k-1)-m_{2i+1}(k-1)=\Delta m > -2\gamma \qquad \text{- inequality 1.}$$

Similarly, $m_{i+N/2}$ (k) is the greater of $[m_{2i+1}(k-1)-\gamma]$ and $[m_{2i}(k-1)+\gamma]$ and the condition of the former quantity being greater than the latter can be re-expressed as the inequality:

$$\Delta m > 2\gamma \qquad \text{- inequality 2.}$$

Figure 2 illustrates a circuit 10 for producing the metrics $m_i(k)$ and $m_{i+N/2}$ (k) from metrics $m_{2i}(k-1)$ and $m_{2i+1}(k-1)$ by performing 2 ACS operations in parallel. The circuit 10 comprises two adders 12 and 14, four selectors 16, 18, 20 and 22 and a selector control unit 24. The inputs to the circuit 10 are the path metrics $m_{2i}(k-1)$ and $m_{2i+1}(k-1)$, the branch metric γ leading from trellis stage k-1 and to trellis stage k a negative version of the branch metric, $-\gamma$. These four inputs are variously supplied to the selector units 16, 18, 20 and 22 and the two path metrics and γ are used as inputs for the selector control unit 24.

Each of the selector units 16, 18, 20 and 22 receives two of the inputs to the circuit and, under the control of a selection signal provided by the selector control unit, passes one of

its two inputs to its output. The inputs to selector unit 16 are the two path metrics. Selector unit 20 has the same inputs. The branch metric γ and the negative version of the branch metric are the two inputs to selector unit 18. Selector unit 22 has the same inputs as selector unit 18. The outputs of selector unit 16 and 18 are added together at adder 12 and the outputs of selector units 20 and 22 are added together at adder 14.

The inputs to the two adders are dictated by the control signals that are supplied to the four selector units. Selector units 16 and 18 are driven by the same control signal 26 and selector units 20 and 22 are likewise driven by a common control signal 28. Each of the control signals 26 and 28 can take only the logical values 1 and 0. The data inputs to the selectors 16, 18, 20 and 22 are all marked either 1 or 0. If the control input to a selector has the value logical 1, then the data input of the selector that is marked 1 is passed to the output of the selector. Otherwise, when the control signal of a selector has the value logical 0, the data input of the selector that is marked logical 0 is passed to the output of the selector.

The output of adder 12 is the metric $m_i(k)$ and takes the value of one of the input path metrics summed with either the positive or negative version of the branch metric, depending upon the value of control signal 26. Control signal 26, after passing through NOT gate 19, also provides an item of traceback data for the calculation of metric $m_i(k)$. The output of adder 14 is the metric $m_{i+N/2}(k)$ and again takes the value of one of the input path metrics summed with either the positive or the negative version of the branch metric, depending upon the value of control signal 28. Control signal 28, after passing through NOT gate 21, also provides an item of traceback data for the calculation of metric $m_{i+N/2}(k)$. The production of the control signals 26 and 28 will now be described with reference to Figure 3, which shows the selector control unit 24 in more detail.

As shown in Figure 3, the selector control unit 24 comprises an adder 30, configured to perform subtraction, a bit shifter 32 and a comparison unit 34. It will be recalled that the three inputs to the selector control unit 24 are the two input path metrics and the branch metric γ. The two path metrics are supplied as the inputs to adder 30 whose output is then the difference in the two path metrics, Δm, as defined in inequalities 1 and 2. The branch

metric γ is supplied to bit shifter 32 which moves the bits in the word representing γ one by place in the direction of increasing significance and appends a zero at the least significant end of the word. In this way, shifter 32 doubles the value of γ.

The quantities Δm and 2γ are supplied to comparison unit 34 in order to test the inequalities 1 and 2. The outputs of the comparison unit 34 are the control signals 26 and 28 for controlling the selector units of Figure 1. Control signal 26 is the result of inequality 1 and control signal 28 is the result of inequality 2. The control signals 26 and 28 take the value of logical 1 if their respective inequalities are true on the basis of the inputs to the selector control unit 24 and the value of control signals 26 and 28 are logical 0 if their respective inequalities are false.

Figure 4 shows the construction of the comparison unit 34. The comparison unit 34 comprises two adders 36 and 38 and two check units 40 and 42. The two inputs to the comparison unit 34, Δm and 2γ, are both supplied to each of the two adders 36 and 38. Adder 36 outputs a signal representing the quantity $\Delta m+2\gamma$. The adder 38 is configured to perform the subtraction $\Delta m-2\gamma$. The check units 40 and 42 each evaluate whether the output of their preceding adder is greater than zero. The implementation used for the check units 40 and 42 will depend upon the convention used to represent binary numbers within the system. For example, the check units 40 and 42 may simply evaluate the state of a sign bit of their respective input words. It will be apparent that the output of check unit 40 indicates whether inequality 1 is true or false and that the output of check unit 42 indicates whether or not inequality 2 is true or false.

Figure 5 shows an alternative construction 34' that can be used for the comparison unit within the selector unit 24. The inputs to the comparison unit 34' are still 2γ and Δm and these signals are again used to produce the two control signals 26 and 28 that indicate whether or not inequalities 1 and 2 are true or false.

The comparison unit 34' comprises an exclusive-or (XOR) gate 44, a multi-bit XOR gate 46, an adder 48, three NOT gates 50, 52 and 54 and two selectors 56 and 58. The input Δm is supplied to one of the inputs of the adder 48. The input 2γ is supplied to an input of the

multi-bit XOR gate 46. The other input of the multi-bit XOR gate 46 is a single-bit control signal 60. The multi-bit XOR gate 46 performs a bitwise XOR operation on the word 2γ and the single bit control signal 60. That is to say, multi-bit XOR gate 46 multiplies each bit of the word 2γ with the single-bit control signal 60 to produce a resultant word which is supplied to the other input of adder 48. The control signal 60 is also supplied to a "carry-in" input of the adder 48.

The most significant bits (MSBs) of the inputs 2γ and Δm are combined at XOR gate 44. The values Δm and 2γ are in twos complement format such that their MSBs are sign bits with logical 1 indicating a negative number and logical 0 indicating a positive number. The output of XOR gate 44 is logical 1 if the values Δm and 2γ have opposite signs and is logical 0 otherwise.

The output of the XOR gate 44 is used to control selectors 56 and 58. Each of the selectors 56 and 58 has a pair of data inputs. One of the data inputs in each pair is marked 1 and the other data input is marked 0. When the output of XOR gate 44 has the value logical 1, the selectors 56 and 58 transfer to their outputs the signals applied to their inputs that are marked 1. If the output of XOR gate 44 has the value logical 0, then the selectors 56 and 58 transfer to their outputs the signals applied to their inputs that are marked 0. The outputs of the selectors 56 and 58 constitute the control signals 26 and 28 respectively.

In addition to being used to control the selectors 56 and 58, the output of the XOR gate 44 is passed through NOT gate 50 to produce control signal 60. The control signal 60 causes the adder 48 to calculate the value $\Delta m+2\gamma$ or $\Delta m-2\gamma$ depending upon whether the control signal 60 has the value logical 0 or logical 1 respectively. The multi-bit XOR gate 46 has no effect on 2γ when the control signal 60 has the value logical 0. Likewise, the control signal 60 does not affect the operation of the adder 48 when it has the state logical 0. When the control signal 60 has the state logical 1, the output of the multi-bit XOR gate 46 is a twos complement word whose algebraic equivalent is $-2\gamma-1$. The adder 48 adds this quantity to Δm but, because the "carry-in" input is now logical 1, the overall calculation performed by the adder 48 is (algebraically) $-2\gamma-1+\Delta m+1 = \Delta m-2\gamma$. Thus, the multi-bit

XOR gate 46 and the adder 48 work together under aegis of control signal 60 to calculate the sum $\Delta m+2\gamma$ or $\Delta m-2\gamma$.

Because the twos complement convention is being used for representing binary numbers in the circuit, the MSB of the result of adder 48 is a sign bit which has the value logical 1 if the adder result is negative and otherwise has the value logical 0. The MSB of the result of adder 48 is then passed through NOT gate 52 to provide an input for terminal "0" of selector 56 and an input for the terminal "1" of selector 58. Terminal "1" of selector 56 is supplied with the MSB of Δm. The MSB of Δm is also passed through NOT gate 54 to provide an input for terminal "0" of selector 58. The output of selector 58 is control signal 26 and has the value logical 1 when inequality 1 is true and logical 0 when the inequality is false. The output of selector 56 is control signal 28 and has the value logical 1 when inequality 2 is true and logical 0 when the inequality is false.

The following truth tables describe the circuit of Figure 5:

MSB of 2γ or $2\gamma<0$?	MSB of Δm or $\Delta m<0$?	Output of XOR 44	Output of NOT 60	Output of Adder 48
1	1	0	1	$\Delta m-2\gamma$
1	0	1	0	$\Delta m+2\gamma$
0	1	1	0	$\Delta m+2\gamma$
0	0	0	1	$\Delta m-2\gamma$

MSB of 2γ or $2\gamma<0$?	MSB of Δm or $\Delta m<0$?	Output of Adder 48	Input of NOT 52	Output of NOT 52
1	1	$\Delta m-2\gamma$	$(\Delta m-2\gamma)<0$?	$(\Delta m-2\gamma)>0$?
1	0	$\Delta m+2\gamma$	$(\Delta m+2\gamma)<0$?	$(\Delta m+2\gamma)>0$?
0	1	$\Delta m+2\gamma$	$(\Delta m+2\gamma)<0$?	$(\Delta m+2\gamma)>0$?
0	0	$\Delta m-2\gamma$	$(\Delta m-2\gamma)<0$?	$(\Delta m-2\gamma)>0$?

MSB of 2γ or $2\gamma<0$?	MSB of Δm or $\Delta m<0$?	Output of XOR 44	Signal 28 or $\Delta m>2\gamma$?	Signal 26 or $\Delta m>-2\gamma$?
1	1	0	$(\Delta m-2\gamma)>0$?	0
1	0	1	1	$(\Delta m+2\gamma)>0$?
0	1	1	0	$(\Delta m+2\gamma)>0$?
0	0	0	$(\Delta m-2\gamma)>0$?	1

CLAIMS

1. A method of calculating a first new path metric from two old path metrics and a branch metric, the method comprising: determining the difference between the two old path metrics; performing a first comparison of the branch metric and said difference; selecting, on the basis of said first comparison, one of the old path metrics for a first combination with the branch metric; and selecting, on the basis of said first comparison, whether said first combination is by addition or subtraction.

2. A method according to claim 1, wherein said first comparison comprises determining whether the result of the first comparison can be determined from the signs of said difference and said branch metric or whether the result of the first comparison needs to be calculated from said difference and said branch metric.

3. A method according to claim 1 or 2, further comprising storing the outcome of the first comparison for use as an item of trace-back information.

4. A method according to claim 1, 2 or 3, wherein said first comparison comprises determining which is the larger of said difference and double the branch metric.

5. A method according to any one of claims 1 to 4, further comprising calculating a second new path metric from the two old path metrics and the branch metric by: performing a second comparison of the branch metric and said difference; selecting, on the basis of said second comparison, one of the old path metrics for a second combination with the branch metric; and selecting, on the basis of said second comparison, whether said second combination is by addition or subtraction.

6. A method according to claim 5, wherein said second comparison comprises determining whether the result of the second comparison can be determined from the signs of said difference and said branch metric or whether the result of the second comparison needs to be calculated from said difference and said branch metric.

7. A method according to claim 5 or 6, further comprising storing the outcome of the second comparison for use as an item of trace-back information.

8. A method according to claim 5, 6 or 7, wherein said second comparison comprises determining which is the larger of said difference and minus double the branch metric.

9. A method according to claim 1, 2 or 3, wherein said first comparison comprises determining which is the larger of said difference and minus double the branch metric.

10. Apparatus for calculating a first new path metric from two old path metrics and a branch metric, the apparatus comprising: subtracting means for determining the difference between the old path metrics; comparing means for performing a first comparison of the branch metric and said difference; and selecting means for selecting, on the basis of said first comparison, one of the old path metrics for a first combination with the branch metric and for selecting, on the basis of said first comparison, whether said first combination is by addition or subtraction.

11. Apparatus according to claim 10, wherein said comparing means is arranged to determine whether the result of the first comparison can be determined from the signs of said difference and said branch metric or whether the result of the first comparison needs to be calculated from said difference and said branch metric.

12. Apparatus according to claim 10 or 11, further comprising storage means for storing the outcome of the first comparison for use as an item of trace-back information.

13. Apparatus according to claim 10, 11 or 12, wherein said first comparison comprises determining which is the larger of said difference and double the branch metric.

14. Apparatus according to any one of claims 10 to 13, wherein said apparatus is arranged to calculate a second new path metric from said old metrics and said branch metric, said comparing means is arranged to perform a second comparison of the branch metric and said difference and the selecting means is arranged to select, on the basis of said second comparison, one of the old path metrics for a second combination with the branch metric and is arranged to select, on the basis of said second comparison, whether said second combination is by addition or subtraction.

15. Apparatus according to claim 14, wherein said comparing means is arranged to determine whether the result of the second comparison can be determined from the

signs of said difference and said branch metrics or whether the result of the first comparison needs to be calculated from said difference and said branch metric.

16. Apparatus according to claim 14 or 15, further comprising storage means for storing the outcome of the second comparison for use as an item of trace-back information.

17. Apparatus according to claim 14, 15 or 16, wherein said second comparison comprises determining which is the larger of said difference and minus double the branch metric.

18. Apparatus according to claim 10, 11 or 12, wherein said first comparison comprises determining which is the larger of said difference and minus double the branch metric.

19. A program for causing data processing apparatus to perform a method according to any one of claims 1 to 9.

20. A method of calculating one or more new path metrics from two old path metrics and a branch metric, the method being substantially as hereinbefore described with reference to the accompanying figures.

21. Apparatus for calculating one or more new path metrics from two old path metrics and a branch metric, the apparatus being substantially as hereinbefore described with reference to the accompanying figures.

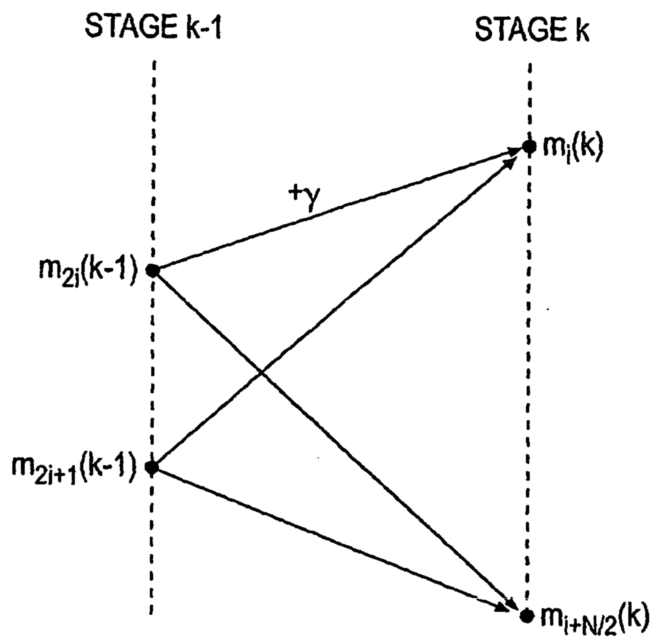
STAGE k-1
STAGE k
$m_i(k)$
$+\gamma$
$m_{2i}(k-1)$
$m_{2i+1}(k-1)$
$m_{i+N/2}(k)$

Fig. 1

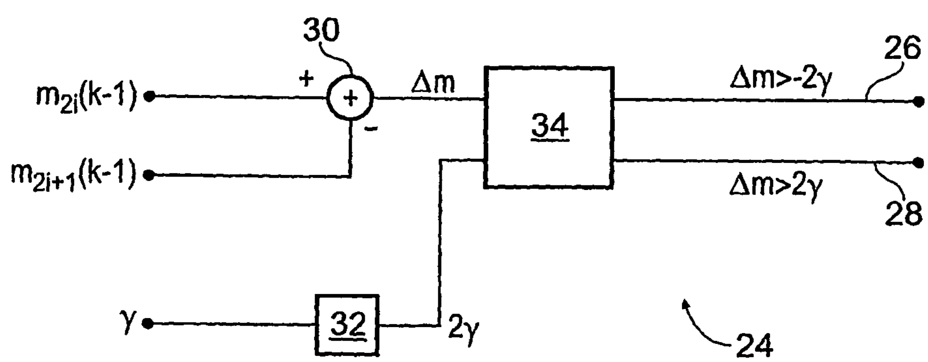
30
26
+
Δm
$\Delta m>-2\gamma$
$m_{2i}(k-1)$
-
34
$m_{2i+1}(k-1)$
$\Delta m>2\gamma$
28
γ
32
2γ
24

Fig. 3

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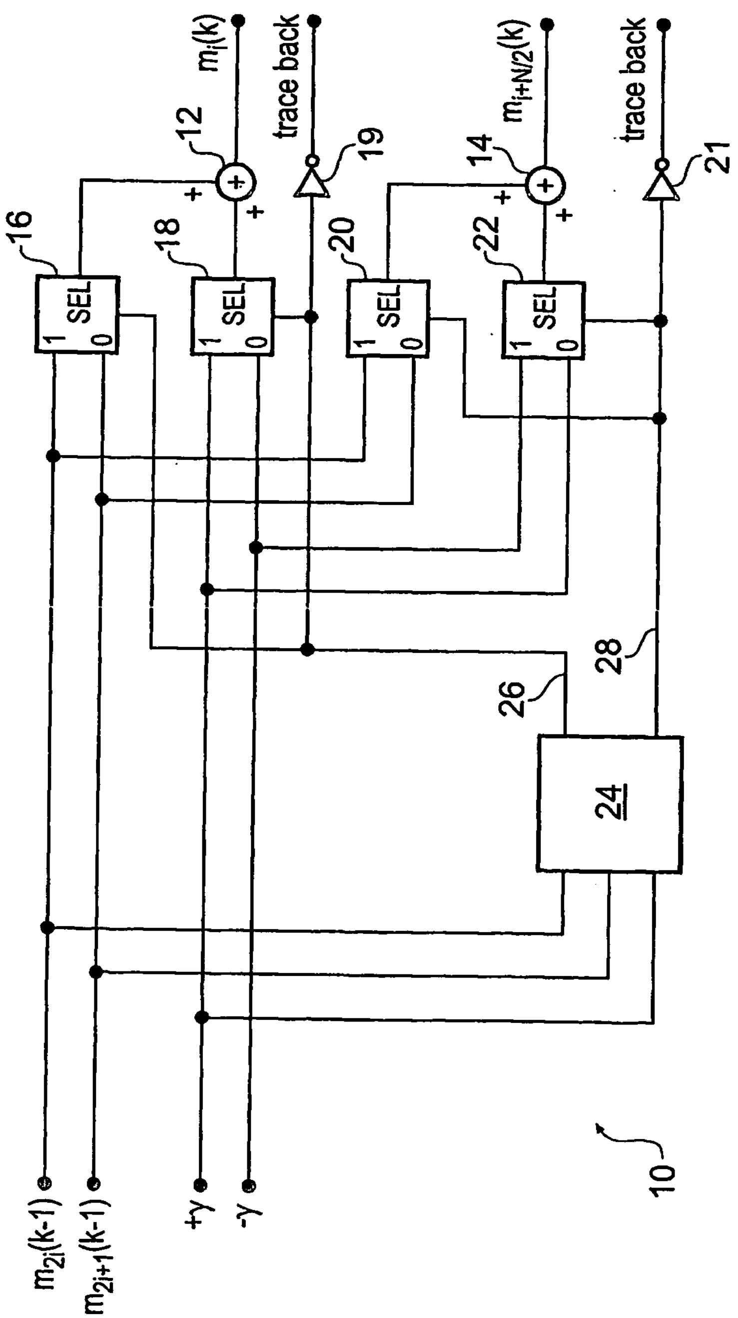

Fig. 2

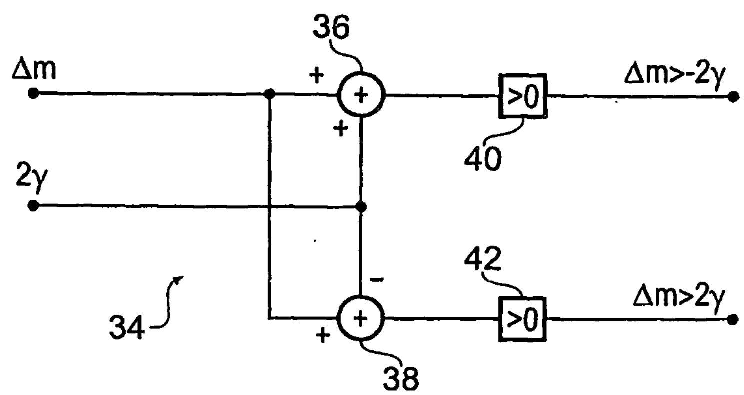
36
Δm
+
+
>0
Δm>-2γ
40
2γ
42
34
-
+
>0
Δm>2γ
38

Fig. 4

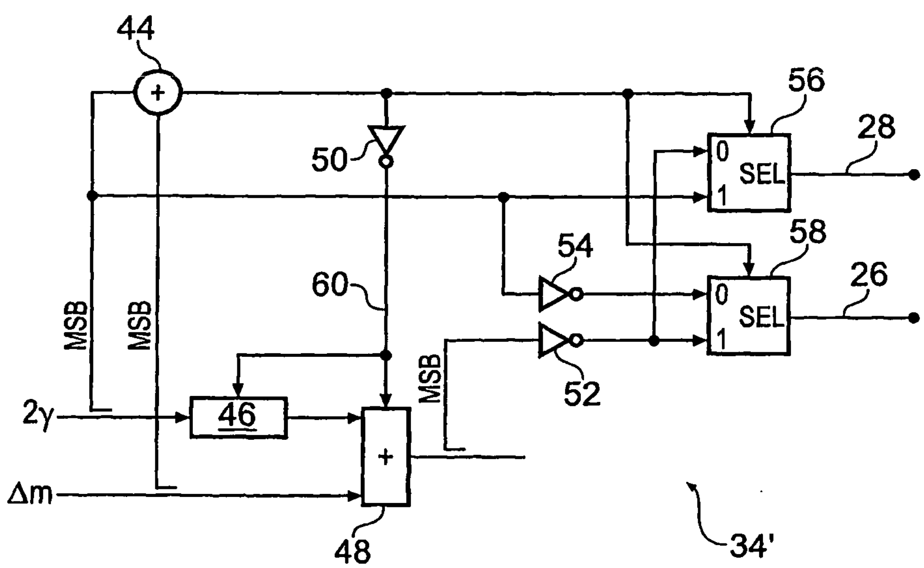
44
56
28
50
0
SEL
1
54
58
26
60
0
SEL
1
MSB
MSB
MSB
52
2γ
46
+
Δm
48
34'

Fig. 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB2004/001770

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M13/41

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PAGE K ET AL: "IMPROVED ARCHITECTURES FOR THE ADD-COMPARE-SELECT OPERATION IN LONG CONSTRAINT LENGTH VITERBI DECODING" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 33, no. 1, January 1998 (1998-01), pages 151-155, XP000766629 ISSN: 0018-9200 section "III. decoupled architecture", Fig. 4	1,3-5, 7-10, 12-14, 16-19
Y		2,6,11, 15
Y	DE 199 37 506 A (INFINEON TECHNOLOGIES AG) 19 April 2001 (2001-04-19) cover page column 6, line 47 - column 8, line 23	2,6,11, 15

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 August 2004	23/08/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Farman, T

Form PCT/ISA/210 (second sheet) (January 2004)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 781 569 A (FOSSORIER M ET AL.) 14 July 1998 (1998-07-14) cover page column 8, line 49 - column 9, line 49	1,3-5, 7-10, 12-14, 16-19
X	US 6 070 263 A (TSUI CHI-YING ET AL) 30 May 2000 (2000-05-30) cover page	1,3-5, 7-10, 12-14, 16-19

INTERNATIONAL SEARCH REPORT

ational application No.
PCT/GB2004/001770

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 20, 21
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 20, 21

These claims do not specify the features to be protected but refer to the description and the drawings. Hence, the features to be searched are not clear.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Int[illegible]nal Application No
PC[illegible]GB2004/001770

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